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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,585	07/01/2003	Kent Oertle	13693US02	5233
23446	7590	08/24/2004	EXAMINER	
MCANDREWS HELD & MALLOY, LTD 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661			LE, DON P	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/611,585

Applicant(s)

OERTLE ET AL.

Examiner

Don P Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/13/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yosefin et al. (US 5,952,875).

3. With respect to claim 1, figure 3 of Yosefin discloses a circuit coupled to an output device (116, N1), the circuit comprising at least one transistor device (N2, N3) adapted to limit a duration of a high voltage across the output device thereby reducing hot carrier injection stress (see abstract).

4. With respect to claim 2, figure 3 of Yosefin discloses two stacked transistor devices (N2, N3).

5. With respect to claims 3 and 4, figure 3 of Yosefin discloses at least one p-channel transistor (160, 170) coupled to the output device.

6. With respect to claims 5 and 6, figure 3 of Yosefin discloses a circuit comprises at least one n-channel output transistor (N2, N3).

7. With respect to claim 7, figure 3 of Yosefin discloses an integrated circuit comprising:

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an output circuit (116, 110); and

a stress circuit (150, N2, N3) coupled to at least said output circuit and adapted to limit a duration of a high voltage across said output circuit thereby reducing hot carrier injection stress.

8. With respect to claim 8, figure 3 of Yosefin discloses the stress circuit comprises stacked transistors (N2, N3).

9. With respect to claim 9, figure 3 of Yosefin discloses an integrated circuit comprising:

an I/O PAD (115);

an output circuit (116, 110) coupled to at least said IO PAD; and

a stress circuit (150, N2, N3) coupled to at least said output circuit and adapted to limit a duration of a high voltage across said output circuit when said output circuit is enabled, thereby reducing stress on said output circuit.

10. With respect to claims 10-12, figure 3 of Yosefin discloses the stress circuit comprises at least one transistor (170, 160).

11. With respect to claims 13-15, figure 3 of Yosefin discloses the stress circuit comprises at least one transistor (N2, N3).

12. With respect to claims 16-21, the methods therein are inherent given the apparatus of Yosefin as shown in the above rejections.

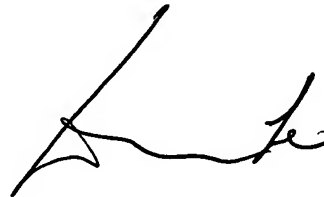
13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P Le whose telephone number is 703-308-4890. The examiner can normally be reached on 7AM - 5PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 703-305-3493. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/17/2004

A handwritten signature in black ink, appearing to read 'Don Le', with a stylized flourish at the end.

DON LE
PRIMARY EXAMINER